A1

the PCI error routine returns and the PCI error is processed in known fashion. If the host bridge did log an error address, firmware uses the firmware maintained PCI resource allocation map to identify the failing PCI slot at 84. As used herein, "failing PCI slot" means that a PCI device has had some type of failure that causes the host bridge to log an error address.

Please delete the Abstract Section of the specification and replace it with the following abstract in clean form. Applicant includes herewith an Attachment for Specification Amendments showing a marked up version of the previous version of the Abstract Section.

ABSTRACT OF THE DISCLOSURE

A2

A method of identifying a failing PCI slot in a computer having a peripheral component interconnect (PCI) system having a host bridge coupling a plurality of PCI slots of a PCI bus to a processor where the computer uses firmware to access the base address registers. A firmware maintained PCI resource allocation map is created which addresses for PCI slots associated with base address registers and sizes of address ranges for these addresses are mapped. The firmware maintained PCI resource allocation map is updated upon the occurrence of at least of firmware being called to execute at least one of a hot plug operation and a PCI configuration space transaction. Upon the host bridge logging an error address due to a failing PCI slot, the failing PCI slot is identified from the information in the firmware maintained PCI resource allocation map.

IN THE CLAIMS

Please amend the claims in accordance with the following rewritten claims in clean form. Applicant includes herewith an Attachment for Claim Amendments showing a marked up version of each amended claim.

A3

1. (Amended) In a computer having a peripheral component interconnect (PCI) system having a host bridge coupling a plurality of PCI slots of a PCI bus to a processor, the computer accessing base address registers with firmware, a method of identifying a failing PCI slot, comprising the steps of:

(a) creating a firmware maintained PCI resource allocation map in which addresses for PCI slots associated with the base address registers and sizes of address ranges for these addresses are mapped;

(b) updating the firmware maintained PCI resource allocation map upon the occurrence of the firmware being called to execute at least one of a hot plug operation and a PCI configuration space transaction; and

(c) upon the host bridge logging an error address due to a failing PCI slot, identifying the failing PCI slot from the information in the firmware maintained PCI resource allocation map.

4. (Amended) The method of claim 1 wherein the step of identifying the failing PCI slot from the information in the firmware maintained PCI resource allocation map includes identifying the failing PCI slot from an address associated with a base address register when the logged error address falls within a known address size range for the address associated with that base address register.

6. (Amended) The method of claim 4 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address the size range for that preceding base address register is unknown.

7. (Amended) The method of claim 6 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address size range for the address associated with that preceding base address register is unknown.

10. (Amended) In a computer having a peripheral component interconnect (PCI) system having a host bridge coupling a plurality of PCI slots of a PCI bus to a processor, the computer accessing base address registers with firmware, a method of identifying a failing PCI slot, comprising the steps of:

(a) creating a firmware maintained PCI resource allocation map in which addresses for PCI slots associated with the base address registers and sizes of address ranges for these addresses are mapped;

(b) upon the occurrence of a hot plug operation for a PCI slot, setting a hot plug flag associated with that PCI slot;

(c) upon the occurrence of at least one of the firmware being called to execute a PCI configuration space transaction and the host bridge logging an error address, invalidating the firmware maintained PCI resource allocation map entries for each PCI slot having its hot flag set; and

(d) upon the host bridge logging an error address due to a failing PCI slot, identifying the failing PCI slot from an address associated with a base address register when the logged error address falls within a known address size range for the address associated with that base address register and identifying the failing PCI slot as unknown when the logged error address falls after a known address size range of an address associated with that base address register preceding the logged error address.

11. (Amended) The method of claim 10 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address size range for the address associated with that preceding base address register is unknown.

13. (Amended) The method of claim 12 wherein the step of identifying the failing PCI slot further includes identifying the failing PCI slot from the address associated with that base address register preceding the logged error address when the address size range for the address associated with that preceding base address register is unknown.